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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	DIETMAR EGGERT WOLFRAM KLUGE	Group Art Unit:	2836
		Examiner:	KIM NGOC HUYNH
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Serial No.:	09/468,015	Atty. Dkt.:	2000.065900/DE0005
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For:	ELECTROSTATIC DISCHARGE PROTECTION NETWORK HAVING DISTRIBUTED COMPONENTS		

4/1/04

APPEAL BRIEF

MAILSTOP APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8	
DATE OF DEPOSIT:	March 23, 2004

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as "FIRST CLASS MAIL" addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Sharon J. Hart
Signature

On December 23, 2003, Appellants filed a Notice of Appeal in response to a Final Office Action dated September 09, 2003, issued in connection with the above-identified application, which was received and stamped by the USPTO Mailroom on December 29, 2003. In support of their appeal, Appellants hereby submit an original and two copies of this Appeal Brief to the Board of Patent Appeals and Interferences in response to the Final Office Action dated September 09, 2003.

The Director is authorized to deduct the fee for filing this Appeal Brief ($330.00) from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/DE0005. Additionally, a check in the amount of $110.00 for a one-month extension for filing this Appeal Brief,

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which is hereby requested by Appellants, is enclosed. Should any additional fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason, the Commissioner is authorized to deduct said fees from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/DE0005. In the event the monies in that account are insufficient, the Commissioner is authorized to withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.065900.

I. REAL PARTY IN INTEREST

The prosecution history reveals that the present patent application was initially assigned to Advanced Micro Devices, Inc. ("AMD") and the real party in interest is AMD.

II. RELATED APPEALS AND INTERFERENCES

Appellants are not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1-20 are pending in the application. Claims 1-3 stand rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 5,529,831 (***Waga***). Claims 1-20 stand rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 5,831,331 (***Lee***) or, in the alternative, under 35 U.S.C. § 103(a) as being obvious over ***Lee*** in view of ***Waga***. The claims currently under consideration, *i.e.*, claims 1-20, are attached as Appendix A.

IV. STATUS OF AMENDMENTS

There were no amendments after the final rejections.

V. SUMMARY OF THE INVENTION

Appellants' inventive methodologies are generally directed to electronic circuits and systems sensitive to electrostatic discharge, and more particularly, to a distributed electrostatic discharge protection network for these electronic circuits and systems operating at radio frequencies.

The present invention provides a system, method and apparatus for providing an electrostatic discharge protection network on an integrated circuit die, a monolithic substrate, and a printed circuit board with or without constant impedance stripline conductors. Various embodiments of the invention include an inductor that has at least one or more turns of a coil, and one or more ESD clamp device connected to the coil(s). More than one coil turn may be associated with one ESD clamp device, and more than one ESD clamp device may be associated with one turn of the coil. The inductor coil may be comprised of any shape or form, and the ESD clamp device may be any other type of transient voltage limiting device.

The inductor portion may be connected in series between an electronic circuit node that is being protected, and an external signal node, which is subject to an ESD event. The ESD clamp device(s) may be connected to the inductor, preferably at each turn of the inductor coil, and to one or both of the common power supply rails. One of the common power supply rails may be at earth ground potential. In addition, it is contemplated and within the scope of the present invention that some of the ESD clamp devices may also be connected between one or more turns of the inductor coil and earth ground.

Figure 2 illustrates a schematic diagram of the ESD protection circuit of the embodiments of the invention. The ESD protection circuit 200 has an external node 206 and an internal node 208. The external node 206 is adapted for connection to circuits having desired signals with undesirable ESD events and the internal node 208 is adapted for connection to circuits needing protection from ESD events. Between the nodes 206 and 208, the ESD protection circuit 200 comprises a series connected inductor 202 between the nodes 206 and 208, wherein the inductor 202 has tapped portions (202a, 202b, 202c and 202d). Parallel or shunt connected ESD clamp devices represented by their parasitic capacitance (204a, 204b, 202c and 204d) are connected to respective inductor 202 tapped portions (202a, 202b, 202c and 202d). The inductor 202 and ESD clamp parasitic capacitance 204 form cascaded "n" sections of a low pass filter network. The series inductance of the inductor coil 202 portions (202a, 202b, 202c and 202d) preferably cancel out the shunt parasitic capacitance (204a, 204b, 202c and 204d) of the ESD clamp device(s) connected thereto for signal frequencies below the low pass filter cutoff frequency. Appropriate selection of inductance 202 and capacitance 204 values for the ESD network 200 may also be used for efficient impedance matching of the signal nodes 206 and 208 to a source and load, respectively.

Figure 3 illustrates a schematic orthogonal view of an embodiment of the invention. The inductor 202 may include one or more turns formed from conductive layers that are coil shaped. These coil shaped conductive layers, (coil turns 202a, 202b, 202c, 202d) are formed on a plurality of insulation layers. Each coil shaped conductive layer is formed on a respective insulation layer (See Figure 4). Various "vias" through the insulation layers are used to connect the different coil shaped conductive layers together by conductive connections. The shape of the

coil may vary, for example, the shape may be round, square, rectangle, triangle, oval, hexagon, octagon and the like. The conductive layer may be made from one or more various metals, such as copper, aluminum, copper alloy and aluminum alloy, or any other conductive material used in the fabrication of an integrated circuit, such as conductive doped polysilicon.

Figure 4 illustrates a cross-section view of the fabricated ESD network 200. An integrated 10 circuit die 400 includes a substrate 410 that contains various doped wells (412a, 412b, 412c and 412d), in which ESD clamp devices have either or both PMOS and NMOS transistors. The PMOS and NMOS transistors of the ESD clamp devices may be connected to the power supply rails, V_{DD} and Vss'.

Insulation layer 414d is formed over the substrate 410 and wells (412a, 412b, 412c, 412d). The insulation layer 414d may also be formed over other conducting and insulation layers proximate to the substrate 410. The coil turn 202d is formed over the insulation layer 414d. Similarly, other insulation layers (414c, 414b, 414a) and coil turns (202c, 202b, 202a) are formed as illustrated in Figure 4. Another insulation layer 416 may be formed over the 20 coil turn 202a for additional circuitry or physical protection of the integrated circuit die.

The ESD clamp devices formed in the wells (412a, 412b, 412c, 412d) may be connected to the coil turns (202a, 202b, 202c, 202d) respectively, through conductive vias (holes) in the insulation layers (414a, 414b, 414c, 414d). The vias are filled with a conductive material such as aluminum. As illustrated in Figure 4, vias 418a pass through insulation layers (414d, 414c, 414b), and connect the ESD clamp device in the well 412a to the coil turn 202a. The vias 418a

do not connect to the other coil turns 202b, 202c and 202d. Vias 418b pass through insulation layers 414d, 414c and 414b, and connect the ESD clamp device in the well 412b to the coil turn 202b. The vias 418b do not connect to the other coil turns (202a, 202c, 202d). Vias 418c pass through insulation layers 414d and 414c, and connect the ESD clamp device in the well 412c to the coil turn 202c. The vias 418c do not connect to the other coil turns (202a, 202b, 202d). Via 418d passes through insulation layer 414d, and connects the ESD clamp device in the well 412d to the coil turn 202d. The internal node 208 connects to circuit logic (not illustrated) of the integrated circuit die, and the external node 206 is adapted for connection to external circuitry. It is also contemplated and within the scope of the invention that the ESD clamp devices may be formed on or attached to each of the insulation layers.

According to another embodiment of the invention, the ESD protection network 15 may be fabricated on a substrate made of either insulation material (*e.g.*, ceramic, glass epoxy, a printed wiring board (PWB), *etc.*), or conductive material (*e.g.*, aluminum, copper, steel brass, *etc.*). A plurality of turns of a coil are formed on a plurality of insulation layers on the substrate. Each one of the insulation layers has one of the coil turns. Vias are formed in each of the plurality of insulation layers, and conductive material is deposited therein for connecting the plurality of coil turns together to form the inductor. The ESD clamp devices may be formed or attached on each of the insulation layers or the ESD clamp devices may be attached to the substrate with connection to the plurality of coil turns made through conductive vias in the various insulation layers on which the coil turns are formed.

Figure 5 illustrates a schematic elevational cross-section view of the ESD network fabricated on a substrate. A substrate 510 may be non-conductive or conductive. If the substrate is conductive, an insulation layer 516 may be used. If the substrate is non-conductive then no insulation layer 516 may be required. A first coil turn 202a is formed over the insulation layer 516 or over the non-conductive substrate 510. The first coil turn 202a is connected to an external input node 206. An insulation layer 514a is formed over the first coil turn 202a. A second coil turn 202b is formed over the insulation layer 514a. Another insulation layer 514b is formed over the second coil turn 202b. A third coil turn 202c is formed over the insulation layer 514b. Still another insulation layer 514c is formed over the third coil turn 10 202c. Yet another insulation layer 514d is formed over the third coil turn 202c. A fourth coil turn 202d is formed over the insulation layer 514c. And another insulation layer 514d is formed over the fourth coil turn 202d. The fourth coil turn 202d is connected to an internal node 208. Any number of coil turns and insulation layers are contemplated and within the scope of the present invention.

ESD clamp devices (512a, 512b, 512c, 512d) may comprise PMOS and NMOS transistors, and may be connected to power supply rails, V_{DD} and Vss, in a fashion similar to the PMOS and NMOS transistor connections illustrated in Figure 1. The ESD clamp devices may be any type of clamp device, connected to a substrate common or earth ground. The ESD clamp devices (512a, 512b, 5l2c, 512d) may be connected to the coil turns (202a, 202b, 202c, 202d), respectively, through conductive vias (holes) in the insulation layers (514a, 514b, 514c, 514d). The vias are filled with a conductive material such as aluminum. As illustrated in Figure 5, vias 518a pass through insulation layers (514d, 514c, 514b), and connect the ESD clamp device 512a to the coil turn 202a. The vias 518a do not connect to the other coil turns (202b, 202c, 202d).

Vias 518b pass through insulation layers (514d, 514c, 514b), and connect the ESD clamp device 512b to the coil turn 202b. The vias 518b do not connect to the other coil turns (202a, 202c, 202d). Vias 518c pass through insulation layers 514d and 514c, and connect the ESD clamp device 512c to the coil turn 202c. The vias 518c do not connect to the other coil turns 202a, 202b and 202d. Via 518d passes through insulation layer 514d, and connects the ESD clamp device 512d to the coil turn 202d. It is also contemplated and within the scope of the invention, that the ESD clamp devices may be formed on each of the insulation layers and attached to the conductive layer coil turns on the insulation layers.

Figures 6 and 7 illustrate a schematic plan view and an elevational view, respectively, of an ESD protection network fabricated on a non-conductive printed circuit board using printed circuit strip line conductors and surface mounted components. The transmission line structures may be used instead of coil shaped structures with the ESD clamp devices. The non-conductive portion of a printed circuit board 610 may be, for example, glass epoxy, TEFLON®, ceramic, glass, *etc.* The printed circuit strip line enables a constant impedance for the signal path. A plurality of turns of a coil 602 are formed on the printed circuit board 610 in a concentric spiral configuration. Conductive vias 612a-612d (plated through holes) may be formed through the printed circuit board 610 at each of the plurality of coil turns, or portions thereof. ESD clamp devices 604a-604d may be attached to respective ones of these vias 612a-612d and to a planar ground plane 712. The ground plane 712 may be located on the face opposite the face on which the plurality of coil turns 602 is located thereon. The ESD clamp devices 604 may be connected to the coil turns 602 by vias 612, and to the planar ground plane 710 by vias 608, or, preferably, by using surface mount techniques. The plurality of coil turns 602 may be tapped with, for

example, the vias 612 at points along the coil 602, which may represent a desired inductance, needed to cancel out the parasitic capacitance of the associated ESD clamp devices 604. The ESD clamp devices 604 may connect to the outer or larger coil turn(s) at less than 360 degrees, and the inner or smaller coil turns 602 at more than 360 degrees, *i.e.*, a multiple turn.

The insulation layers between the coil turns of the inductor may preferably be very thin so that the turns of the coil are close together, thus, improving the magnetic coupling therebetween and increasing the effective inductance for a given size coil diameter. Referring to Figure 8, a schematic orthogonal view of the coil portion of Figure 3 and a core having magnetic properties to increase the inductance of the coil 202 is illustrated. A core 820 comprising a material of high magnetic permeability may be located within the coil 202 so as to further increase the effective inductance value for a given size of coil structure. This material may be, for example, iron, iron oxide, ferrite ceramic, ferrous oxide, or other materials that increase the effective inductance of the inductor coil.

VI. ISSUE ON APPEAL

Claims 1-20 are pending in the application.

Appellants respectfully request that the Board review and overturn the following rejections present in this case. The following issues are presented on appeal in this case:

1. Whether claims 1-3 are anticipated under U.S.C. § 102(a) by U.S. Patent No. 5,529,831 (***Waga***).

2. Whether claims 1-20 are anticipated under 35 U.S.C. § 102(a) by U.S. Patent No. 5,831,331 (***Lee***) or, in the alternative, whether claims 1-20 are obvious under 35 U.S.C. § 103(a) over ***Lee*** in view of ***Waga***.

VII. GROUPING OF THE CLAIMS

For each of the issues presented above, the appealed claims 1-3 can be considered to stand or fall together; the appealed claims 3-17 can be considered to stand or fall together; and the appealed claims 18-20 can be considered to stand or fall together.

VIII. ARGUMENT

Appellants respectfully assert that ***Waga***, ***Lee***, or their combination do not disclose, suggest, or make obvious all of the elements of claims of the present invention. Therefore, claims 1-20 are allowable.

A. Claims 1-3 are not anticipated under U.S.C. § 102(a) by U.S. Patent No. 5,529,831 (*Waga*)

In the Final Office Action dated September 2, 2003, the Examiner rejected claims 1-3 under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 5,529,831 (***Waga***). Appellants respectfully traverse this rejection.

The Examiner asserted that although ***Waga*** does not mention electro-static discharge (ESD) devices, the capacitors 26 in ***Waga*** anticipate the ESD devices in the claims of the present invention. Appellants respectfully disagree. ***Waga*** does not disclose or suggest any devices directed toward discharge of electro-static energy. The apparatus with the reference number

"26" in ***Waga*** is a dielectric layer 26 in a thin film device 21 (see col. 8, lines 1-15 and Figure 9). The thin film device 21 serves a "distributed constant-type L-C device" (see col. 8, lines 27-28). In contrast to the Examiner's assertions, Appellants respectfully assert ***Waga*** does not disclose a capacitor that may be used to anticipate an ESD device. ***Waga*** does not even mention a "capacitor 26"; additionally, ***Waga*** does not mention, disclose, or suggest a capacitor that may be used to anticipate an ESD clamp (structurally or functionally). The reference number "26" that the Examiner cites as "capacitor 26" merely refers to a dielectric layer 26 in a thin film device 21 (col. 8, lines 1-15). The apparatus cited by the Examiner using the reference number "26" does not function as an ESD device (as called for by claim 1 of the present invention), and it is structurally different, contrary to the Examiner's assertions in the Final Office Action dated September 02, 2003, and in the Advisory Action dated December 04, 2003.

Merely providing an L-C circuit will not anticipate an ESD clamp called for by claim 1 of the present invention. Additionally, ***Waga*** does not disclose any devices that have a parasitic capacitance, which is called for by claim 1 of the present invention (*e.g.*, claims 1 and 18 calls for an ESD clamp having a parasitic capacitance). Therefore, ***Waga*** cannot, and does not, teach, anticipate, or suggest all of the elements of independent claim 1.

Waga is directed to a thin film device 21 that includes a magnetic substrate and spiral coils. The L-C filter provided by ***Waga*** (see Figure 10) is directed towards eliminating noise in input signals (see col. 8, lines 26-33). However, the circuitry provided by ***Waga*** does not provide for electro-static discharge (ESD) protection. ***Waga*** does not disclose a plurality of ESD clamp devices, as called for by claims 1 and 18 of the present invention. Merely providing the

L-C filter (Figure 10) and a coil (Figure 11) would not teach the plurality of ESD clamp devices having a parasitic capacitance, which is not even mentioned by ***Waga***. ***Waga*** merely provides a thin film equivalent circuit that provides a L-C filter to eliminate noise, it does not provide a plurality of ESD clamp devices having parasitic capacitance (see col. 4, line 64-col 5, line 3; col. 8, lines 27-47). ***Waga*** does not disclose connecting ESD clamp devices (that have parasitic capacitances) to a corresponding turn of a plurality of turns of an inductor, as called for by the claims of the present invention. Therefore, ***Waga*** does not teach all of the elements called for by independent claim 1 of the present invention. Additionally, independent claim 4 calls for an apparatus that comprises the plurality of ESD clamp devices described above, therefore, for at least the reasons cited above, claim 4 is also allowable, since all of its elements are not taught, disclosed, or made obvious by ***Waga***. Furthermore, independent claim 18 calls for providing a plurality of electrostatic discharge (ESD) clamp devices and connecting them such that a low pass filter is created. For at least the reasons cited above, the subject matter of claim 18 is also not disclosed, taught, or made obvious by ***Waga***.

Independent claims 1, 4, and 18 are allowable for at least the reasons cited above. Additionally, claims 2-3, 5-17, and 19-20, which depend from independent claims 1, 4, and 18, respectively, are also allowable for at least the reasons cited above.

B. Claims 1-20 are not anticipated under 35 U.S.C. § 102(a) by U.S. Patent No. 5,831,331 (*Lee*). Additionally, claims 1-20 are not obvious under 35 U.S.C. § 103(a) over Lee in view of *Waga*.

Appellants respectfully assert that neither ***Lee***, ***Waga***, nor their combination disclose, suggest or make obvious, all of the elements of the present invention. Appellants believe ***Lee***

does not read on the claimed invention because ***Lee*** does not disclose all of the elements called for by the claimed invention. Contrary to the Examiner's assertion (in the Advisory Action dated December 04, 2003), that ***Lee*** shows the identical structure of Appellants' invention, Appellants respectfully assert that ***Lee*** does not show or suggest the identical structure of Appellants' invention. The Examiner did not offer arguments or evidence to support such an assertion. Contrary to the Examiner's statement in the Advisory Action dated December 04, 2003, Appellants did not assert that ***Lee*** does not read on the claimed invention merely because ***Lee*** does not use the same terminology as preferred by Appellants. Appellants assert that ***Lee*** does not read on the claimed invention because ***Lee*** does not disclose, suggest, or make obvious the structure or functions called for by claims of the present invention.

Lee is directed to an inductor having multiple turns disposed one above another in respective metallization layers of an IC. Although ***Lee*** may teach or suggest a "stacked" coil configuration, ***Lee*** does not teach or suggest the use of more than one ESD clamp device with the plurality of coils. ***Lee*** does not disclose the plurality of ESD clamps that have parasitic capacitance, as called for by claims 1, 4, and 18 of the present invention. Therefore, ***Lee*** does not disclose or teach all of the elements called for by independent claims 1, 4, and 18 of the present invention.

Additionally, the claims of the present invention call for at least one via for forming an inductor coil. Although ***Lee*** discloses using vias that connect various inductive coils, ***Lee*** does not disclose or suggest using at least one via for forming an inductor coil for generating an inductance for a low pass filter, as called for by claims 1, 4, and 18 of the present invention.

Therefore, ***Lee*** does not disclose or teach all of the elements called for by independent claims 1, 4, and 18 of the present invention.

Furthermore, claims 1-20 are not obvious under 35 U.S.C. § 103(a) over ***Lee*** in view of ***Waga***. This is true since ***Waga*** does not compensate for the deficit of ***Lee***. As described above, ***Waga*** does not teach or make obvious the ESD clamp called for by the claims of the present invention. ***Waga*** does not disclose or suggest any capacitors that may be used to anticipate the ESD clamp called for by claims 1, 4, and 18. ***Lee*** does not compensate for this deficit. Neither the disclosure of ***Waga*** nor the disclosure of ***Lee*** disclose or suggest a low-pass filter using parasitic capacitance. The Examiner suggested that ***Lee*** does not disclose a plurality of ESD devices, but suggests that this deficit is made up stating that ESD or capacitance formed between the conductive layers are adequate to anticipate the present invention. Appellants respectfully disagree. Neither ***Lee*** nor ***Waga*** disclose or suggest a plurality of ESD devices that inherently exist between conductive layers. Even though ***Lee*** and ***Waga*** disclose multiple turns, they do not disclose a plurality of ESD clamps. Therefore, structures called for by claims 1, 4 and 18 (all as amended) are not taught, disclosed, or suggested by ***Lee***, ***Waga***, or their combination. For this reason alone, the independent claims of the present invention, which call for a plurality of ESD devices, are allowable. Accordingly, the combination of ***Waga*** and ***Lee*** does not anticipate all of the elements of independent claims 1 and 18 of the present invention. Hence, independent claims 1, 4, and 18 of the present invention are allowable.

Independent claims 1, 4, and 18 are allowable for at least the reasons cited above. Additionally, claims 2-3, 5-17 and 19-20, which depend from independent claims 1, 4, and 18, respectively, are also allowable for at least the reasons cited above.

IX. CONCLUSION

In view of the foregoing remarks, it is respectfully submitted that the Examiner erred in not allowing all claims pending in the present application, claims 1-20, over the prior art of record. In view of the foregoing, Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the decision rejecting claims 1-20 and direct the Examiner to pass the case to issue. The undersigned attorney may be contacted at (713) 934-4069 with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,

WILLIAMS, MORGAN & AMERSON, P.C.
CUSTOMER NO. 23720

Date: March 23, 2004

By: _____

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APPENDIX A

1. (Previously presented) An electrostatic discharge (ESD) protection network, comprising:

an inductor having a plurality of turns in the shape of a coil, the plurality of turns having an inductance;

a plurality of electrostatic discharge (ESD) clamp devices, each one of said plurality of ESD clamp devices having a parasitic capacitance, said plurality of ESD clamp devices being connected to a corresponding one of said plurality of turns of said inductor, the inductance of said turns and the parasitic capacitance of said ESD clamp devices thereby forming a low pass filter and;

at least one via for forming an inductor coil for generating an inductance for said low pass filter.

2. (Previously presented) The ESD protection network of claim 1, wherein said plurality of turns and said plurality of ESD clamp devices are fabricated on a surface selected from the group consisting of a substrate and an integrated circuit die.

3. (Previously presented) The ESD protection network of claim 1, wherein said plurality of turns and said plurality of ESD clamp devices are fabricated on an integrated circuit die.

4. (Previously presented) An integrated circuit apparatus having an electrostatic discharge (ESD) protection network, said apparatus comprising:

an integrated circuit substrate;

a first insulation layer over a face of said integrated circuit substrate;

a plurality of conductive layers, each of the plurality of conductive layers in the shape of a coil turn, the coil turn having a first and second end;

a plurality of insulation layers interleaved between the plurality of conductive layers;

a one of said plurality of conductive layers proximate to said first insulation layer and the other ones of said plurality of conductive layers stacked over the one with said plurality of insulation layers interleaved therebetween;

a plurality of vias in the plurality of insulation layers, the plurality of vias connecting adjacent ones of the coil turns of said plurality of conductive layers, thereby forming an inductor coil for generating an inductance for said low pass filter; and

a plurality of electrostatic discharge (ESD) clamp devices, each one of said plurality of ESD clamp devices having a parasitic capacitance, said plurality of ESD clamp devices being connected to a corresponding one of the coil turns of said plurality of conductive layers, thereby forming a low pass filter.

5. (Original) The apparatus of claim 4, w herein respective ones of said plurality of conductive vias connect the second ends of each one of the coil turns of said plurality of conductive layers to the first ends of each of the adjacent ones of the coil turns of said plurality of conductive layers, thereby forming the inductor coil.

6. (Original) The apparatus of claim 5, wherein each of the respective ones of said plurality of conductive vias is at least one via.

7. (Original) The apparatus of claim 5, wherein each of the respective ones of said plurality of conductive vias is two or more vias so as to reduce electrical connection resistance thereof.

8. (Original) The apparatus of claim 4, wherein the shape of the coil turns of said plurality of conductive layers is selected from the group consisting of round, square, rectangle, triangle, oval, hexagon and octagon.

9. (Original) The apparatus of claim 4, wherein said plurality of conductive layers is made of metal.

10. (Original) The apparatus of claim 9, wherein the metal is selected from the group consisting of copper, aluminum, copper alloy and aluminum alloy.

11. (Original) The apparatus of claim 1, wherein said plurality of conductive layers is made of conductive doped polysilicon.

12. (Original) The apparatus of claim 4, further comprising a magnetic material interposed concentrically inside of an inner diameter of the coil turns of said plurality of conductive layers so as to increase the inductance thereof.

13. (Original) The apparatus of claim 12, wherein the magnetic material is selected from the group consisting of iron, iron oxide, ferrite ceramic and ferrous oxide.

14. (Original) The apparatus of claim 4, wherein at least one ESD claim device is connected to each one of said plurality of conductive layers.

15. (Original) The apparatus of claim 4, wherein at least one of said plurality of conductive layers is connected to a one of said plurality of ESD claim devices.

16. (Original) The apparatus of claim 4, wherein said plurality of ESD clamp devices are fabricated in said integrated circuit substrate and connected to said plurality of conductive layers with vias through said plurality of insulation layers.

17. (Original) The apparatus of claim 4, wherein said plurality of ESD claim devices are fabricated on at least one of said plurality of insulation layers and connected to said plurality of conductive layers with vias through said plurality of insulation layers.

18. (Previously presented) A method for providing an electrostatic discharge (ESD) protection network, comprising:

forming a plurality of conductive layers and a plurality of insulation layers, wherein said plurality of conductive layers and said plurality of insulation layers are interleaved, wherein each of the conductive layers is formed in the shape of a coil

turn having an inductance such that such that each of the coil turns has a first and a second end;

forming a plurality of vias in said plurality of insulation layers, the plurality of vias being located between the ends of adjacent coil turns wherein conductive material is formed in said plurality of vias thereby connecting the first end of one coil turn to the second end of the adjacent coil turn for generating an inductance for said low pass filter;

providing a plurality of electrostatic discharge (ESD) clamp devices, each one of said plurality of ESD clamp devices having a parasitic capacitance; and

connecting said plurality of ESD clamp devices to a corresponding one of the coil turns of said plurality of conductive layers, thereby forming a low pass filter.

19. (Original) The method of claim 18, wherein the step of connecting said plurality of ESD clamp device comprises the step of connecting at least one ESD clamp device to each one of said plurality of conductive layers.

20. (Original) The method of claim 18, wherein the step of connecting said plurality of ESD clamp devices comprises the step of connecting at least one of said plurality of conductive layers is to a one of said plurality of ESD clamp devices.